Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **14EC2068** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VHDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | List the various VHDL operators and explain its operation in VHDL. | CO1 | 10 |
| b. | Construct full adder using VHDL structural modelling. | CO2 | 10 |
| (OR) | | | | |
| 2. | a. | Show and explain a typical design flow process for designing VLSI IC circuits. | CO1 | 10 |
| b. | Design a combinational circuit for the following truth table using VHDL behavioral modeling using IF statement.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | A | B | C | D | Y | | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 1 | 1 | | 0 | 0 | 1 | 0 | 0 | | 0 | 0 | 1 | 1 | 1 | | 0 | 1 | 0 | 0 | 1 | | 0 | 1 | 0 | 1 | 0 | | 0 | 1 | 1 | 0 | 1 | | 0 | 1 | 1 | 1 | 1 | | 1 | 0 | 0 | 0 | 1 | | 1 | 0 | 0 | 1 | 1 | | 1 | 0 | 1 | 0 | 0 | | 1 | 0 | 1 | 1 | 0 | | 1 | 1 | 0 | 0 | 1 | | 1 | 1 | 0 | 1 | 0 | | 1 | 1 | 1 | 0 | 1 | | 1 | 1 | 1 | 1 | 1 | | CO2 | 10 |
|  |  |  |  |  |
| 3. | a. | Design the following combinational circuit using VHDL Data flow modeling. Each gate has a 5 ns delay and the inverter has a 2 ns delay. | CO2 | 10 |
| b. | Show the syntax of selected signal assignment statement and conditional signal assignment statement. | CO1 | 5 |
| c. | Design a combinational circuit for the following expression using VHDL | CO2 | 5 |
| (OR) | | | | |
| 4. | a. | TYPE count is RANGE 0 TO 127;  TYPE states IS (idle, decision,read,write);  TYPE word IS ARRAY(15 DOWNTO 0) OF bit;  count'left = ---------- count'right = ----------  count'high = ----------count'low = ----------  count'length = ----------  states'left = -------- states'right = -------  states'high = ---------states'low = ----------  states'length = ---------  word'left = ---------- word'right = ----------  word'high = ----------word'low =----------  word'length = ---------- | CO1 | 15 |
| b. | Construct D flip flop using VHDL. | CO2 | 5 |
|  |  |  |  |  |
| 5. | a. | Develop a 4X1 multiplxer VHDL test bench | CO3 | 10 |
| b. | Explain different delay models in VHDL | CO1 | 10 |
| (OR) | | | | |
| 6. | a. | Explain Different Loop statements in VHDL | CO1 | 10 |
| b. | Design 4 bit updown counter using VHDL | CO2 | 10 |
|  |  |  |  |  |
| 7. |  | Write ALU VHDL program for the following operation  **ALU**  **ARITHMETIC**  **LOGICAL**  L  M  LSEL  A  B  A SEL  AOUT  LOUT   |  |  |  |  | | --- | --- | --- | --- | | **ASEL** | **AOUT** | **LSEL** | **LOUT** | | ADD | A+B | OR1 | L OR M | | SUB | A-B | AND1 | L AND M | | MUL | A\*B | NAND1 | L NAND M | | DIV | A/B | NOR1 | L NOR M | | AMIX | (A+B)\*(A-B) | EXOR1 | L XOR M | | BMIX | (A\*B)+A | LMIX | (L OR M) AND L | | CO2 | 20 |
| (OR) | | | | |
| 8. |  | Design the following circuit using VHDL  Image result for moore model state diagram | CO2 | 20 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | Compare function and procedure in sub program. | CO3 | 2 |
| b. | Develop a VHDL package for full adder circuit. | CO3 | 15 |
| c. | With one example Show how the generics are used in VHDL program. | CO3 | 3 |